1. Overview

R9A06G037 is a high performance NB-PLC (Narrow Band Power Line Communication) modem LSI. R9A06G037 integrates a high performance DSP core and a MCU core (ARM® Cortex™-M3). The DSP core mainly handles PLC PHY layer protocol and the ARM core handles the upper layer protocol. R9A06G037 can support a variety of PLC protocols such as G3-PLC (Cenelec, ARIB and FCC), PRIME and many others.

1.1 Features

- High performance DSP
  - Handles PLC PHY layer and other real time operations
  - 276MHz maximum clock frequency
  - 128KB of instruction RAM and 128KB of data RAM
  - Dedicated instructions for Vitervi, read Solomon and others
- MCU(ARM® Cortex™-M3)
  - Handls PLC MAC layer and upper layer operation
  - 138 MHz maximum clock frequency
  - 512KB of RAM
  - AES128 encryption and decryption hardware engine
  - CRC hardware engine
- 16KB of shared memory
- Analog Front End circuit
  - DAC
    - 12MHz, 12bit
  - Tx filter
    - 3rd order filter
    - 150KHz for Cenelec and 600KHz for ARIB and FCC cutoff frequency
  - Rx variable amplifier
    - -18dB to +60dB dynamic range with 2dB step
    - Auto Gain Control controlled by DSP
  - ADC
    - Delta – sigma type of ADC
    - 11bits ENOB
- Programmable and Multiplexed General-Purpose Input/Output (GPIO) Pins
    - UART(2ch), CSI(2ch), IIC, Serial-ROM-IF(Single/Dual/Quad), PWM(2ch) and GPIO(16)
- Integrated regulator
    - 3.3V input and 1.1V output
- Power Supply Voltage: 3.3V
- PKG : 64-pin QFN, 9mm x 9mm, 0.5mm pitch
- Operating Temperature
  - -40 to +85℃

1.2 System configuration

R9A06G037 provides outstanding communication performance and the most cost-effective solution over PLC networks. Fig. 1.1 shows a system configuration example of R9A06G037.

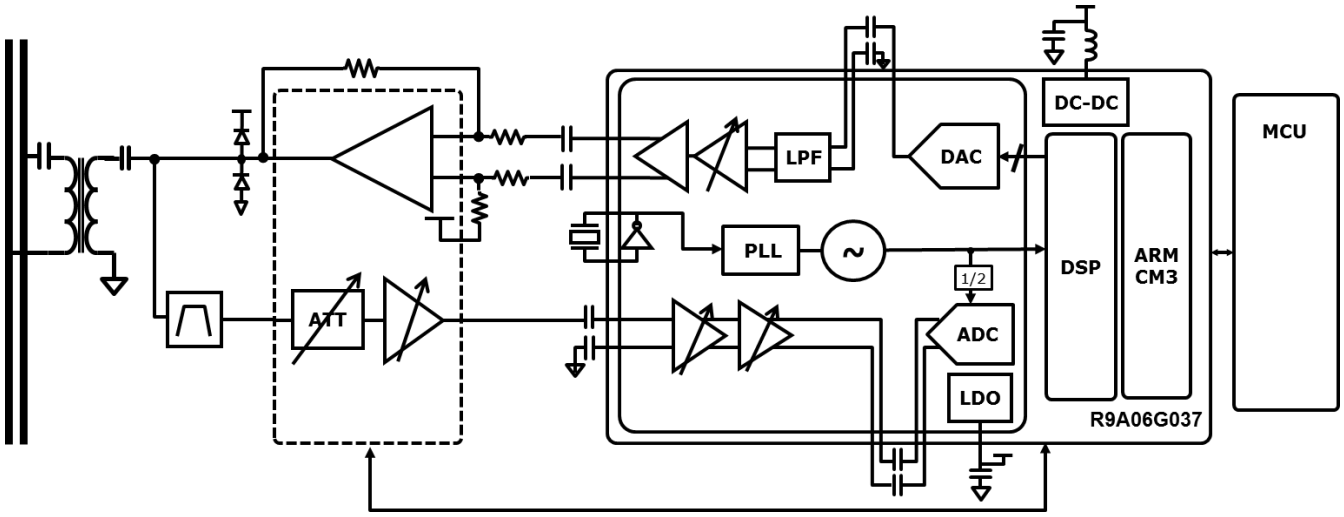


Fig. 1.1 R9A06G037 sytem configuration example with single ended analog input and differential ended

2. Pin functions

2.1 Pin assignment

Fig.2.1 shows the pin assignment of R9A06G037.

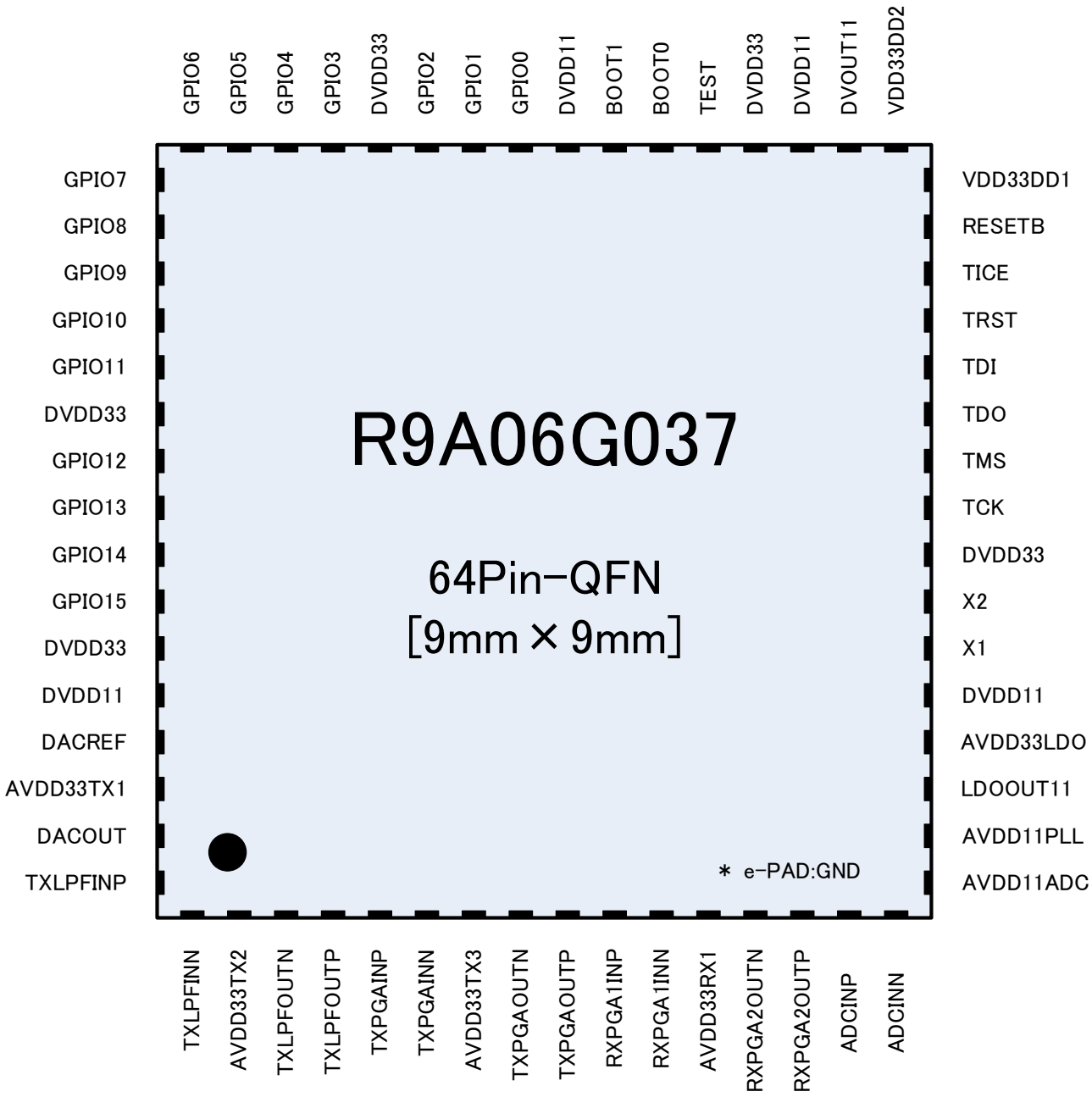


Fig. 2.1 Pin assignment

2.2 Pin description

2.2.1 System clock & Reset

Pin name	I/O	BUFTYPE	Pin No	Functions
X1	I	—	22	External X'tal oscillator input, f=16MHz. ※When use as external clock input mode(BOOT1=LOW),connect to GND.
X2	O/I	—	23	External X'tal oscillator output ※When use as external clock input mode(BOOT1=LOW), X2 is clock input terminal.
RESETB	I	Schmitt/PU	31	System Reset with an internal pullup resister

PU: With a 50KΩ internal pullup resister

2.2.2 BOOT I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
BOOT0	I	PU	38	・Boot mode selection with an internal pullup resister BOOT0=High → UART_S-IF BOOT0=Low → SROM-IF UART_S-IF RXD：GPIO0 TXD：GPIO1 SROM-IF SIO1/MISO ：GPIO3 SSB ：GPIO4 SCK ：GPIO5 SIO0/MOSI ：GPIO6 (SIO2：GPIO7) (SIO3：GPIO8)
BOOT1	I	PU	39	・Clock operation mode selection with an internal pullup resister BOOT1=High: Oscillation mode BOOT1=Low : External clock input mode

PU: With a 50KΩ internal pullup resister

2.2.3 GPIO I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
GPIO0	I/O	B-4/6/8/12mA Schmitt/PU/PD	41	・General-purpose input/output [0]
GPIO1	I/O	B-4/6/8/12mA Schmitt/PU/PD	42	・General-purpose input/output [1]
GPIO2	I/O	B-4/6/8/12mA Schmitt/PU/PD	43	・General-purpose input/output [2]
GPIO3	I/O	B-4/6/8/12mA Schmitt/PU/PD	45	・General-purpose input/output [3]
GPIO4	I/O	B-4/6/8/12mA Schmitt/PU/PD	46	・General-purpose input/output [4]
GPIO5	I/O	B-4/6/8/12mA Schmitt/PU/PD	47	・General-purpose input/output [5]
GPIO6	I/O	B-4/6/8/12mA Schmitt/PU/PD	48	・General-purpose input/output [6]
GPIO7	I/O	B-4/6/8/12mA Schmitt/PU/PD	49	・General-purpose input/output [7]
GPIO8	I/O	B-4/6/8/12mA Schmitt/PU/PD	50	・General-purpose input/output [8]
GPIO9	I/O	B-4/6/8/12mA Schmitt/PU/PD	51	・General-purpose input/output [9]
GPIO10	I/O	B-4/6/8/12mA Schmitt/PU/PD	52	・General-purpose input/output [10]
GPIO11	I/O	B-4/6/8/12mA Schmitt/PU/PD	53	・General-purpose input/output [11]
GPIO12	I/O	B-4/6/8/12mA Schmitt/PU/PD	55	・General-purpose input/output [12]
GPIO13	I/O	B-4/6/8/12mA Schmitt/PU/PD	56	・General-purpose input/output [13]
GPIO14	I/O	B-4/6/8/12mA Schmitt/PU/PD	57	・General-purpose input/output [14]
GPIO15	I/O	B-4/6/8/12mA Schmitt/PU/PD	58	・General-purpose input/output [15]

PD: With a 50KΩ internal pulldown resister / PU: With a 50KΩ internal pullup resister
Default buffer type is 8mA/PU (with 50KΩ internal pullup resister).
The function of each GPIO can be selected from UART, CSI, IIC, Serial-ROM-IF (Single/Dual/Quad), PWM or GPIO.

2.2.4 DAC I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
DACREF	-	Analog	61	Bypass capacitance
DACOUT	O	Analog	63	DAC output signal

2.2.5 TX_LPF I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
TXLPFINP	I	Analog	64	TX_LPF input signal (+)
TXLPFINN	I	Analog	1	TX_LPF input signal (-)
TXLPFOUTN	O	Analog	3	TX_LPF output signal (+)
TXLPFOUTP	O	Analog	4	TX_LPF output signal (+)

2.2.6 TX_PGA I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
TXPGAINP	I	Analog	5	TX_PGA input signal (+)
TXPGAINN	I	Analog	6	TX_PGA input signal (-)
TXPGAOUTN	O	Analog	8	TX_PGA output signal (-)
TXPGAOUTP	O	Analog	9	TX_PGA output signal (+)

2.2.7 RX_PGA I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
RXPGA1INP	I	Analog	10	RX_PGA input signal (+)
RXPGA1INN	I	Analog	11	RX_PGA input signal (-)
RXPGA2OUTN	O	Analog	13	RX_PGA output signal (-)
RXPGA2OUTP	O	Analog	14	RX_PGA output signal (+)

2.2.8 ADC I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
ADCINP	I	Analog	15	ADC input signal (+)
ADCINN	I	Analog	16	ADC input signal (-)

2.2.9 Power/other

Pin name	I/O	BUFTYPE	Pin No	Functions
DVDD33	I	―	24 36 44 54 59	IO buffer power supply 3.3V
VDD33DD1	I	Analog	32	DC-DC control power supply 3.3V
VDD33DD2	I	Analog	33	DC-DC drive power supply 3.3V
DVDD11	I	―	21 35 40 60	Internal core power supply 1.1V
DVOUT11	O	Analog	34	DC-DC power output (3.3V PWM) [1.1V can be generated with an external LC filter circuit]
GND	-	―	-	Common GND ※back face(ePAD)
AVDD33TX1	I	Analog	62	DAC analog power supply 3.3V
AVDD33TX2	I	Analog	2	TX_LPF analog power supply3.3V
AVDD33TX3	I	Analog	7	TX_PGA analog power supply 3.3V
AVDD33LDO	I	Analog	20	LDO analog power supply 3.3V
LDOOUT11	O	Analog	19	LDO power output 1.1V
AVDD33RX1	I	Analog	12	RX_PGA analog power supply 3.3V
AVDD11ADC	I	Analog	17	ADC analog power supply 1.1V
AVDD11PLL	I	Analog	18	PLL analog power supply 1.1V
AVDD33TX1	I	Analog	62	DAC analog power supply 3.3V

2.2.10 Debug I/F

R9A06G037 incorporates two-wire serial mode (SWD) dedicated for JTAG and ARM as debugging IF.

Pin name	I/O	BUFTYPE	Pin No	Functions
TCK	I	PU	25	JTAG Clock (SWDCLK)
TRST	I	PU	29	JTAG Reset (NA)
TMS	I	PU	26	JTAG Test Mode (SWD)
TDI	I	PU	28	JTAG input Data (NA)
TDO	O	4/6/8/12mA PU/PD	27	JTAG output Data (SWV) Default: 8mA/PU with 50K Ω internal pull up resister
TICE	I	PU	30	JTAG selection H: ARM CM3 (Default) L: DSP

PD: With a 50KΩ internal pulldown resister. / PU: With a 50KΩ internal pullup resister.

2.2.11 LSI TEST I/F

Pin name	I/O	BUFTYPE	Pin No	Functions
TEST	I	PD	37	LSI TEST selection Connect to GND via a resistor. (1KΩ~5.1KΩ) during normal operation.

PD: With a 50KΩ internal pulldown resister.

3. Function overview

3.1 Block diagram

Fig. 3.1 shows the block diagram of R9A06G037. R9A06G037 inegrates ARM domain, DSP domain and AFE domain. It also has built-in shared memory, GPIO and regulator.

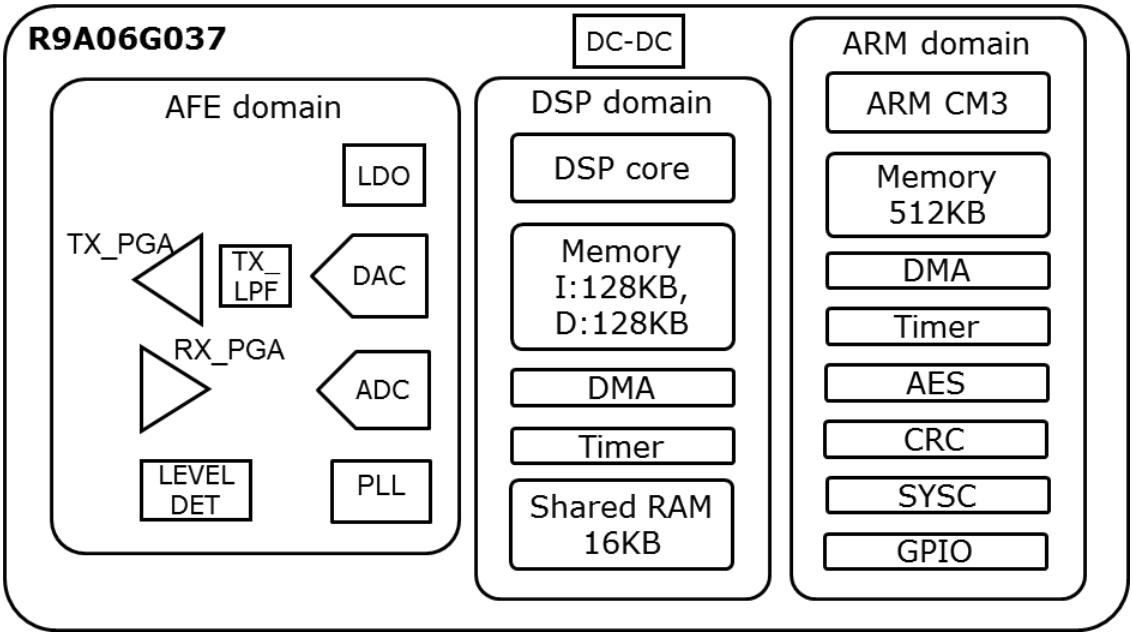


Fig. 3.1 R9A06G037 block diagram

3.2 ARM domain

3.2.1 ARM CM3

R9A06G037 integrates ARM® Cortex™-M3. Maximum operational clock frequency is 138MHz. The range of clock frequency is from 4.3MHz to 138MHz. The clock is generated by system clock controller and can be changed dynamically.

3.2.2 DMA

The DMA that is integrated in ARM domain can support 4-channel DMA requests. Each transfer size can be set to ranging from 1 to 128bytes.

3.2.3 Memory

ARM domain includes 512Kbytes of RAM. ARM® Cortex™-M3 in ARM domain can also access the shared 16KB RAM in DSP domain for communicatin between ARM domain and DSP domain.

3.2.4 AES encription and decription

ARM domain has an AES encryption and decryption function that supports 128bits key length. The function has three operation modes (ECB, CBC and CCM).

3.2.5 CRC

ARM domain integrates a CRC computation hardware core. The CRC computation hardware core supports 4 modes (CRC32, CRC16-ITU, CRC1-IBM and CRC8).

3.2.6 Timer

ARM domain has a timer block with 9 channel 32bits counter. Timer interval can be set to a value from 1 to 4,294,967,296 (32bit timers) using a selected clock frequency. When the timer is equal to the value of the compare register, interrupt can be generated.

3.2.7 WDT

ARM domain has a Watch Dog Timer composed of the counter in 32bits. Alarm is asserted in every cycle that was set to the counter of WDT. After the first alarm is asserted, software does not clear WDT before the second asserting of alarm by the counter overflows so that WDT reset signal is generated.

3.2.8 System control (SYSC)

ARM domain has the system controller (SYSC) that manages the clock frequency for each block and the reset control.The clock frequency can be changed dynamically. The clock frequency to DSP domain can be controlled by DSP.

3.2.9 GPIO

The function of GPIO pins are selected from UART, CSI, IIC, Serial ROM-IF (Single/Dual/Quad), PWM or GPIO. DSP also accesses the GPIO pins.

3.3 DSP domain

3.3.1 DSP

DSP domain has a high performance DSP. The DSP supports a variety of hardware-based instructions for Viterbi, Read Solomon and other functions.The DSP can effectively realize various power line communication PHY layer with the hardware-based instructions. The maximum clock frequency of the DSP is 276MHz. The clock frequency can be changed from 4.3MHz to 276MHz dynamically. When the clock frequency is managed according to the load of the DSP, the power consumption can be optimized.

3.3.2 DMA

The DMA that is integrated in ARM domain can support 4-channel DMA requests. Each transfer size can be set to ranging from 1 to 128bytes.

3.3.3 Memory

DSP domain includes 128KBytes of instruction RAM and 128KBytes of data RAM. DSP domain also includes 16KBytes of ROM for the communication between ARM® Cortex™-M3 and the DSP.

3.3.4 Timer

DSP domain has a timer block with 9 channel 32bits counter. Timer interval can be set to a value from 1 to 4,294,967,296 (32bit timers) using a selected clock frequency. When the timer is equal to the value of the compare register, interrupt can be generated.

3.3.5 Watch Dog Timer (WDT)

DSP domain has a Watch Dog Timer composed of the counter in 32bits. Alarm is asserted in every cycle that was set to the counter of WDT. After the first alarm is asserted, software does not clear WDT before the second asserting of alarm by the counter overflows so that WDT reset signal is generated.

3.4 AFE (Analog Front End) domain

3.4.1 DAC

Digital - Analog converter. Sampling frequency is 12MHz. Resolution is 12bits.

3.4.2 TX_LPF

Low Pass Filter that deletes the image signal from output of DAC. Cut off frequency is selectable from 150KHz for Cenelec and 600KHz for ARIB/FCC.

3.4.3 TX_PGA

Transmit Programable Gain Amplifier that can adjust ouput signal gain. The gain can be programmable with 3dB step from -3dB to +18dB.

3.4.4 RX_PGA

Receive Programable Amplifier that can adjust received signal gain. The gain can be programmable with 2dB step from -18dB to +60dB. DSP computes the received signal level optimization. DSP controls the gain of RX PGA based on the computation. Then, AGC (Auto Gain Control) that controls the amplitude of the recived signal automatically can be realized.

3.4.5 ADC

Delta-sigma type Analog-Digital converter. The maximum smapling frequency is 138MHz. SINAD≧68dB can be achieved in the PLC signal band less than 500KHz.

3.4.6 Received signal level detector

Received signal level detector. It detects the received signal power level even though the the received signal is clipped at RX PGA. The detected level is selectable from -26dBm, -20dBm, or -14dBm.

3.5 Regulator

3.5.1 DC-DC

Swithing DC-DC regulator. The regulator generates 1.1V power supply from 3.3V power supply. 1.1V power supply can be supplied to the digital circuit in R9A06G037.

3.5.2 LDO

Low Drop Off Series regulator. The regulator generates 1.1V power supply from 3.3V power supply. 1.1V power supply can be supplied to the digital circuit in R9A06G037.

3.6 Clock supply mode

R9A06G037 can choose a clock supply mode from “X1 oscillation mode” or “X2 external clock input mode” by BOOT1 terminal setting. When BOOT1 termial is open, “X1 oscillation mode” is chosen for LSI internal pullup register.

BOOT1	Clock mode	X1terminal	X2 terminal
Open（Pullup）	X1 oscillation mode	Connect crystal unit/ceramic resonator	
GND short	X2 external clock input mode	GND short	External clock source

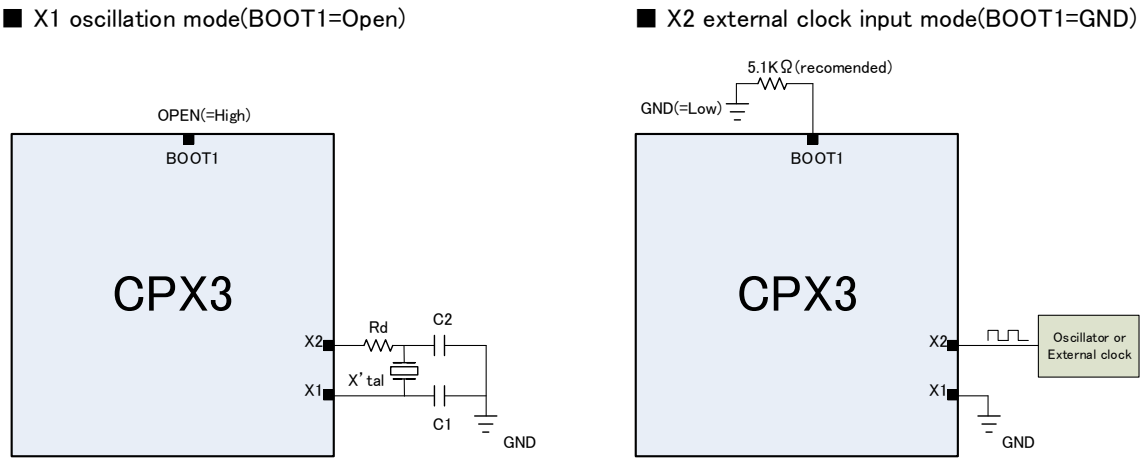


Fig. 3.2 Clock supply mode

4. Electrical characteristics

4.1 Absolute Maximum Rating

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	VDD, AVDD	1.1V	-0.45～+1.8	V
		3.3V	-0.5～+4.6	V
Input/output Voltages	Vi/Vo	$V_I/V_O<V_{DD}+0.5V$	-0.5～+4.6	V
Ouput current (3.3V buffer)	Io	4mA/6mA/8mA/12mA	9.28/13.92/18.56/23.20	mA

Caution:

Product quality may be impaired if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, therefore, the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

4.2 Recommended Operating conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage (digital)	VDD	1.1V	1.0	1.1	1.2	V
		3.3V	3.0	3.3	3.6	V
Supply voltage (analog)	AVDD	1.1V	1.05	1.1	1.2	V
		3.3V	3.0	3.3	3.6	V
Negative trigger input voltage	V_N	3.3V operation	0.7		1.9	V
Positive trigger input voltage	V_P	3.3V operation	0.9		2.1	V
Hysteresis Voltage	V_H	3.3V operation	0.2		1.4	V
Low level input voltage	V_{IL}	3.3V operation	-0.3		0.8	V
High level input voltage	V_{IH}	3.3V operation	2.0		VDD+0.3	V
An input rise/ fall time (data)	t_{rid}	-	0		200	ns
	t_{fid}	-	0		200	ns
An input rise/ fall time (clock)	t_{ric}	-	0		4	ns
	t_{fic}	-	0		4	ns
An input rise/ fall time (Schmidt)	t_{ris}	-	0		1	ms
	t_{fis}	-	0		1	ms
Operating ambient temperature	T_a		-40		+85	℃

4.3 Reset and Power Up/Down Sequence

4.3.1 Reset Sequence

Fig. 4.1 shows R9A06G037 reset sequence. Do not de-assert RESETB before keeping the low level for at least 1ms from the moment IO power supply reaches 0.9 IO_VDD.

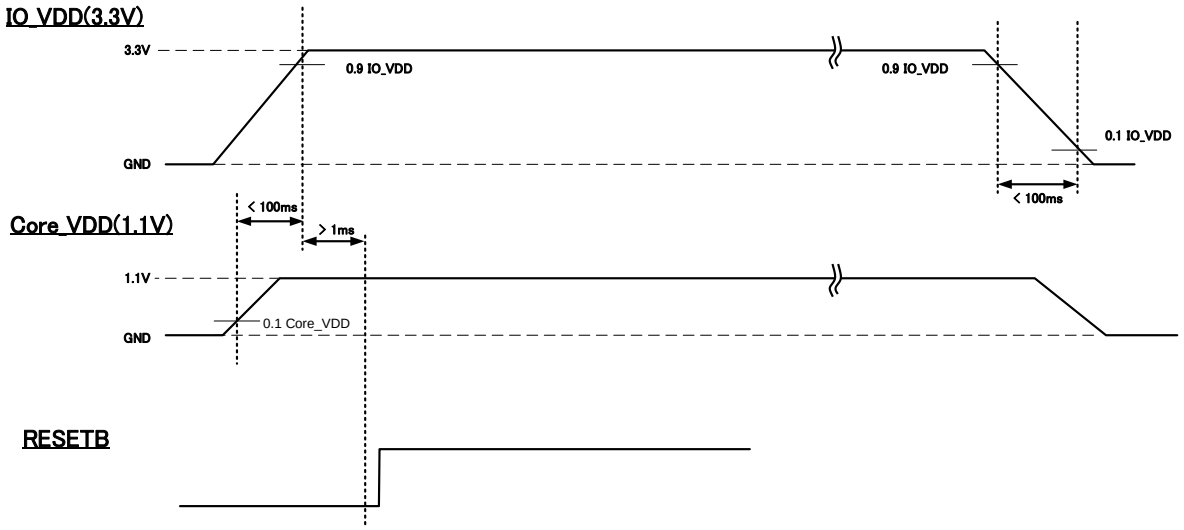


Fig. 4.1 Reset sequence

4.3.2 Power Up/Down Sequence

Fig. 4.2 shows the power up/down sequence. It is recommended that the time which elapses from the start of power-supply rise (either the internal or I/O power supply) until both power supplies are stabilized should be within 100ms, regardless of the order of power supply.

Power supply voltage is recommended to rise from 0.1 VDD to 0.9 VDD within 100ms.

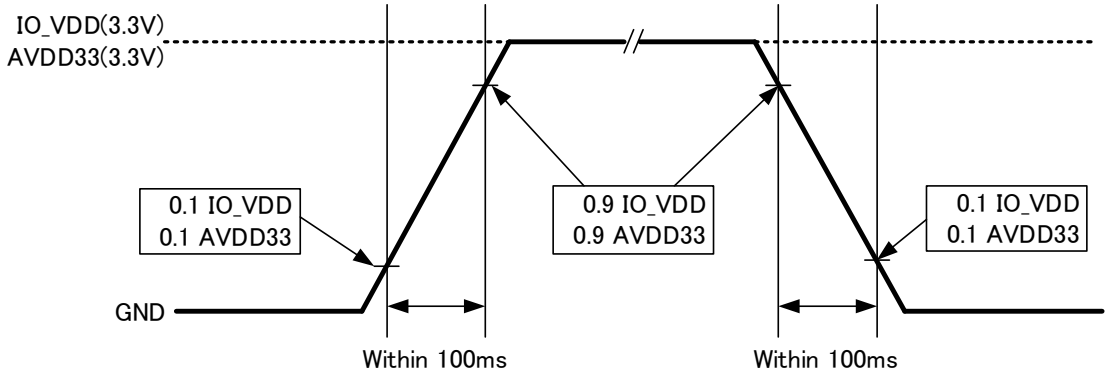


Fig. 4.2 Power up and down sequence

4.3.3 System clock Timing

Symbol	Parameter	MIN	TYP	MAX	Units
$F_{XTALcyc}$	X'tal mode: X1/X2 X'tal clock frequency		16 ±25ppm		MHz
F_{EXcyc}	External clock input mode: X2 input clock frequency		16 ±25ppm		MHz

Clock timing

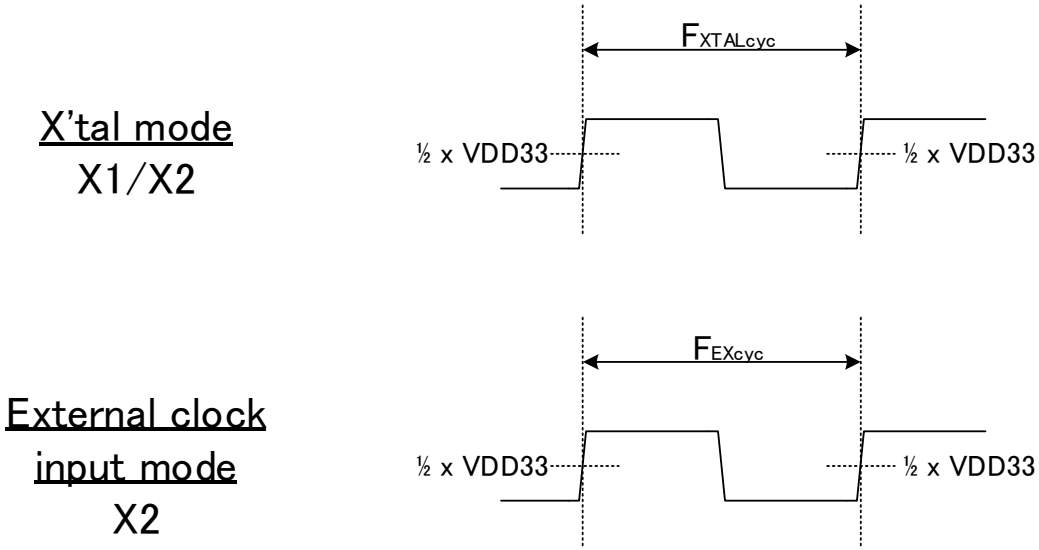


Fig. 4.3 System clock timing cart

4.4 DC Characteristics

DC Characteristics (VDD=3.3+/-0.3V, T_a = −40~+85 ℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output short circuit current (Note 1)	I_{OS}	Vo=GND	-	-	-250	mA
Input leakage current	I_{IL}	Normal input Vin=GND	-	-	-5	µA
	I_{IH}	Normal input Vin=IOVDD	-	-	5	µA
	I_{PU}	Pull up resister Vin=GND	-46.2	-	-102.9	µA
	I_{PD}	Pull down resister Vin=IOVDD	46.2	-	102.9	µA
Output leakage current	I_{OZL}	Vo=GND	-	-	-5	µA
	I_{OZH}	Vo=IOVDD	-	-	5	µA
Low level output current	I_{OL}	VOL=0.4V 4mA/6mA/8mA/12mA	4/6/7.8/9.5	-	-	mA
High level output current	I_{OH}	VOH=2.4V 4mA/6mA/8mA/12mA	4/6/7.8/9.5	-	-	mA
Pull up resister	R_{pu}	Vin=GND	35	50	65	KΩ
Pull down resister	R_{pd}	Vin=IOVDD	35	50	65	KΩ
Low level output voltage	V_{OL}	Iol=0mA	-	-	0.1	V
High level output voltage	V_{OH}	Ioh=0mA	IOVDD-0.1	-	-	V

Note1. Output short circuit time is 1 second or less and applies to only one termination of LSI.

4.5 AC Characterstics

4.5.1 UART

Fig. 4.4 shows UART timing chart.

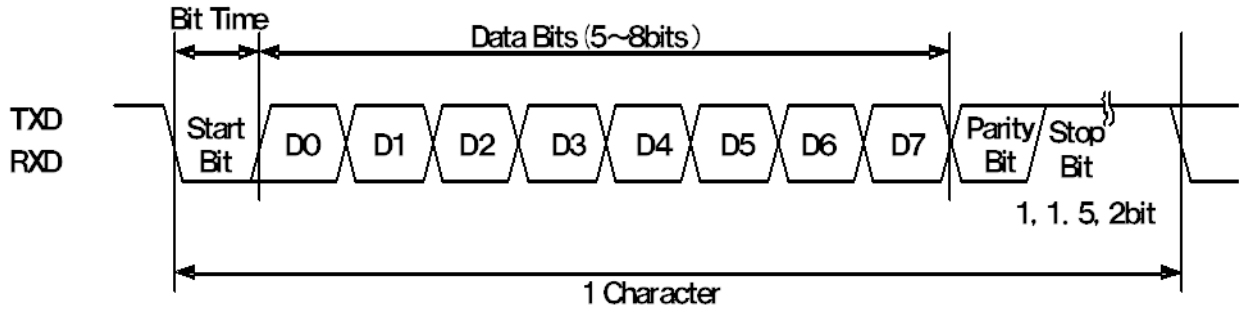


Fig. 4.4 UART timing cart

4.5.2 SerialROM

Fig. 4.5 shows SerialROM timing chart.

Latency 1 mode (Default)

Symbol	Parameter	MIN	TYP	MAX	Units
F_{CLK}	Clock frequency	2.875 (T_{SCK} = 347.8ns)		46 (T_{SCK} = 21.7ns)	MHz
T_{SCKH}, T_{SCKL}	Clock high, low time	T_{SCK} x 0.45		T_{SCK} x 0.55	ns
T_{DD}	Output data（MI,MO,CS）valid time from clock	0		5	ns
T_{DS}	Input data（MI,MO）setup time	11			ns
T_{DH}	Input data（MI,MO）hold time	1			ns

Latency 2 mode

Symbol	Parameter	MIN	TYP	MAX	Units
F_{CLK}	Clock frequency	2.875 (T_{SCK} = 347.8ns)		69 (T_{SCK} = 14.5ns)	MHz
T_{SCKH}, T_{SCKL}	Clock high, low time	T_{SCK} x 0.45		T_{SCK} x 0.55	ns
T_{DD}	Output data（MI,MO,CS）valid time from clock	0		5	ns
T_{DS}	Input data（MI,MO）setup time	5			ns
T_{DH}	Input data（MI,MO）hold time	1			ns

Remark:

Latency 2 mode supports clock frequency up to 69MHz. However, the number of read cycle for serial data increases by one cycle compared to latency 1 mode.

Single/Dual/Quad mode

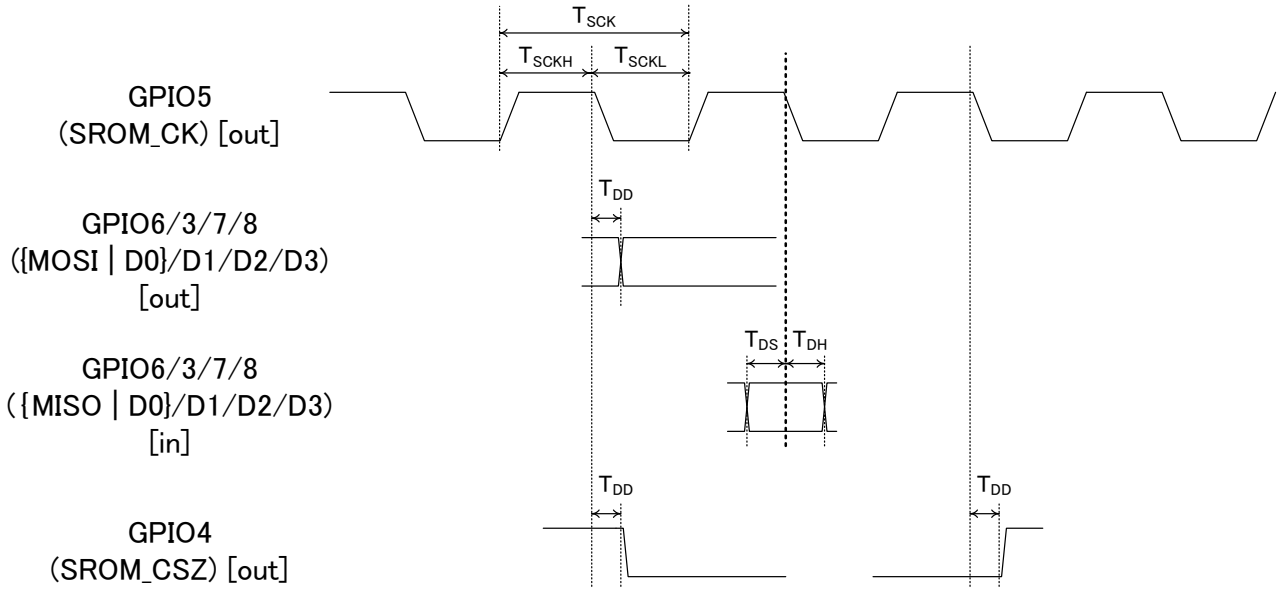


Fig. 4.5 SerialROM timing chart

4.5.3 Current consumption

VDD	MIN.	TYP.	MAX.	Unit
VDD33		25		mA
VDD11		65		mA

Condition: VDD33=3.3+/-0.3V, VDD11＝1.1+/-0.1V,
Renesas reference board used, DSP=276MHz, receive mode with G3-Cenelec-A.

4.6 Analog block characteristic

4.6.1 DC Characteristics

Pin No.	Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
2	Power Supply Voltage		AVDD33TX2	3.0	3.3	3.6	V
7	Power Supply Voltage		AVDD33TX3	3.0	3.3	3.6	V
20	Power Supply Voltage		AVDD33LDO	3.0	3.3	3.6	V
12	Power Supply Voltage		AVDD33RX1	3.0	3.3	3.6	V
17	Power Supply Voltage		AVDD11ADC	1.05	1.1	1.2	V
18	Power Supply Voltage		AVDD11PLL	1.0	1.1	1.2	V
62	Power Supply Voltage		AVDD33TX1	3.0	3.3	3.6	V

4.6.2 Performance Characteristics

4.6.2.1 Receiver block

(a) RX-PGA interface

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Input voltage range	Differential	V_i	60u		3.0	Vp-p
Input Frequency		F_{sig}	30		500	kHz
Dynamic range (Voltage gain range)		DR		78		dB
Gain adjustment step		D_{STEP}		2		dB
Input -1dB Compression	G_V=-14dB,fsig=30kHz, Differential	$P_{in\ 1dB}$	2.8	3.3		Vp-p
Maximum Voltage Gain	f_{sig}=500kHz	G_{V_max}		60		dB
Minimum Voltage Gain	f_{sig}=500kHz	G_{V_min}		-18		dB
Input Impedance		Z_i		1		kΩ
Output load Impedance		R_L		20		kΩ

(b) ADC interface

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Input voltage range	Differential	V_{sig}			800	mVp-p
Input Frequency		F_{sig}			500	kHz
Sampling frequency		F_{CLK}	-	138	-	MHz
ENOB		ENOB	11	-	-	Bit
SINAD		SINAD	68	-	-	dB
Input Impedance		Z_i		20		kΩ

4.6.2.2 Transmit block

(a) DAC interface

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Output voltage range	$Z_L \geqq 10k\Omega$	V_o		1.30		Vp-p
Sampling Frequency		F_{CLK}			12	MHz
Resolution		RES	12			Bit
Differential Nonlinearity (DNL)		DNL			+/-0.5	LSB
Integral Nonlinearity (INL)		INL			+/-3.0	LSB
Output Load resistance		Z_L		10		KΩ

(b) TX-PGA interface

Normal drive mode

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Input voltage range	Differential	V_I		1.30		Vp-p
Input Frequency		f_{sig}	10		500	kHz
Dynamic Range (VoltageGain Range)		DR		21		dB
Gain Control Step		D_{STEP}		3		
Maximum Voltage Gain	f_{sig}=500kHz, differential mode	G_{v_max}		18		dB
Minimum Voltage Gain	f_{sig}=500kHz, differential mode	G_{v_min}		-3		dB
Output-1dB Compression	G_V=+6dB ,f_{sig}=500kHz,Z_L=390Ω	P_1	2			Vp-p
Harmonic Distortion	Gv=+6dB, f_{sig}=100kHz V_I=0.45Vp-p, Z_L=390Ω	HD	-65	-70		dBc
Input Impedance		Z_I		5		kΩ
Output load Impedance		Z_L		390		Ω

High drive mode

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Input voltage range	Differential	V_I		1.30		Vp-p
Input Frequency		f_{sig}	10		500	kHz
Dynamic Range (VoltageGain Range)		DR		21		dB
Gain Control Step		D_{STEP}		3		

Maximum Voltage Gain	f_{sig}=500kHz, differential mode	G_{v_max}		18		dB
Minimum Voltage Gain	f_{sig}=500kHz, differential mode	G_{v_min}		-3		dB
Output-1dB Compression	G_V=+3dB ,fsig=500kHz, Z_L=50Ω	P_1	0.5			Vp-p
Harmonic Distortion	Gv=+3dB, f_{sig}=100kHz, V_I=0.35Vp-p, Z_L=50Ω	HD	-60	-70		dBc
Input Impedance		Z_I		5		kΩ
Output load Impedance		Z_L		50		Ω

(c) TX-LPF interface

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Cutoff Frequency	G3-CENELEC	F_c		150		kHz
	G3-ARIB/FCC			600		kHz
Outband Attenuation	1.9MHz (G3-CENELEC)	D_{ATTE}		-65		dB
	11.5MHz (G3-ARIB/FCC)			-75		dB
Output-1dB Compression		P_1	3			Vp-p

4.6.2.3 Power Supply Regulator

(a) DC/DC

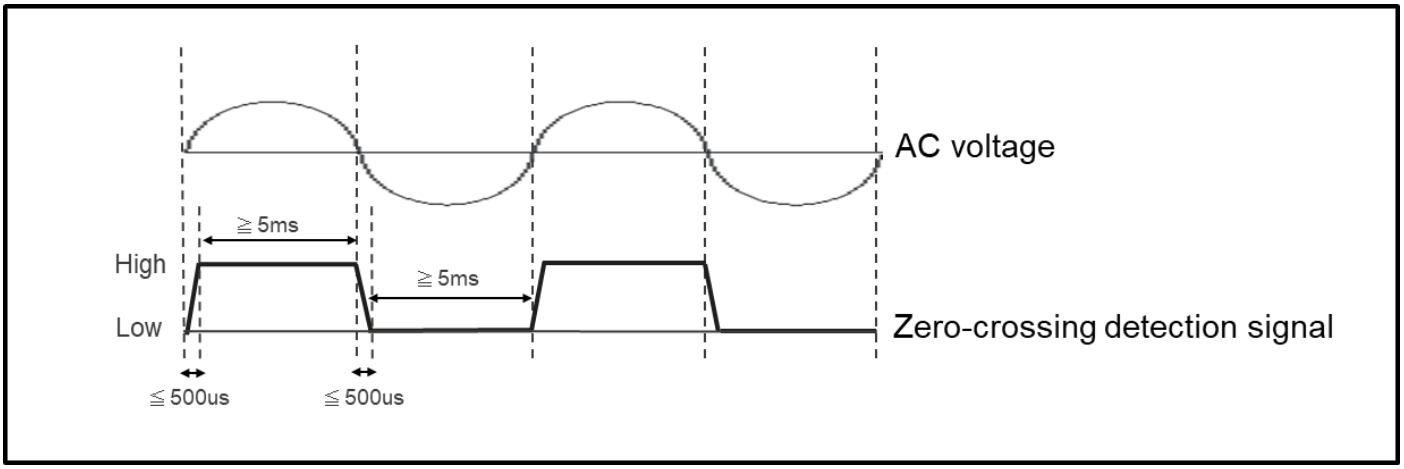
Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Output voltage		V_o	1.0	1.1	1.2	V
Output load current		I_{OL}			240	mA

(b) LDO

Parameter	Conditions	Symbol	MIN	TYP	MAX	Unit
Output voltage		V_o	1.05	1.1	1.2	V
Output load current		I_{OL}			30	mA

4.7 Zero-crossing Detection

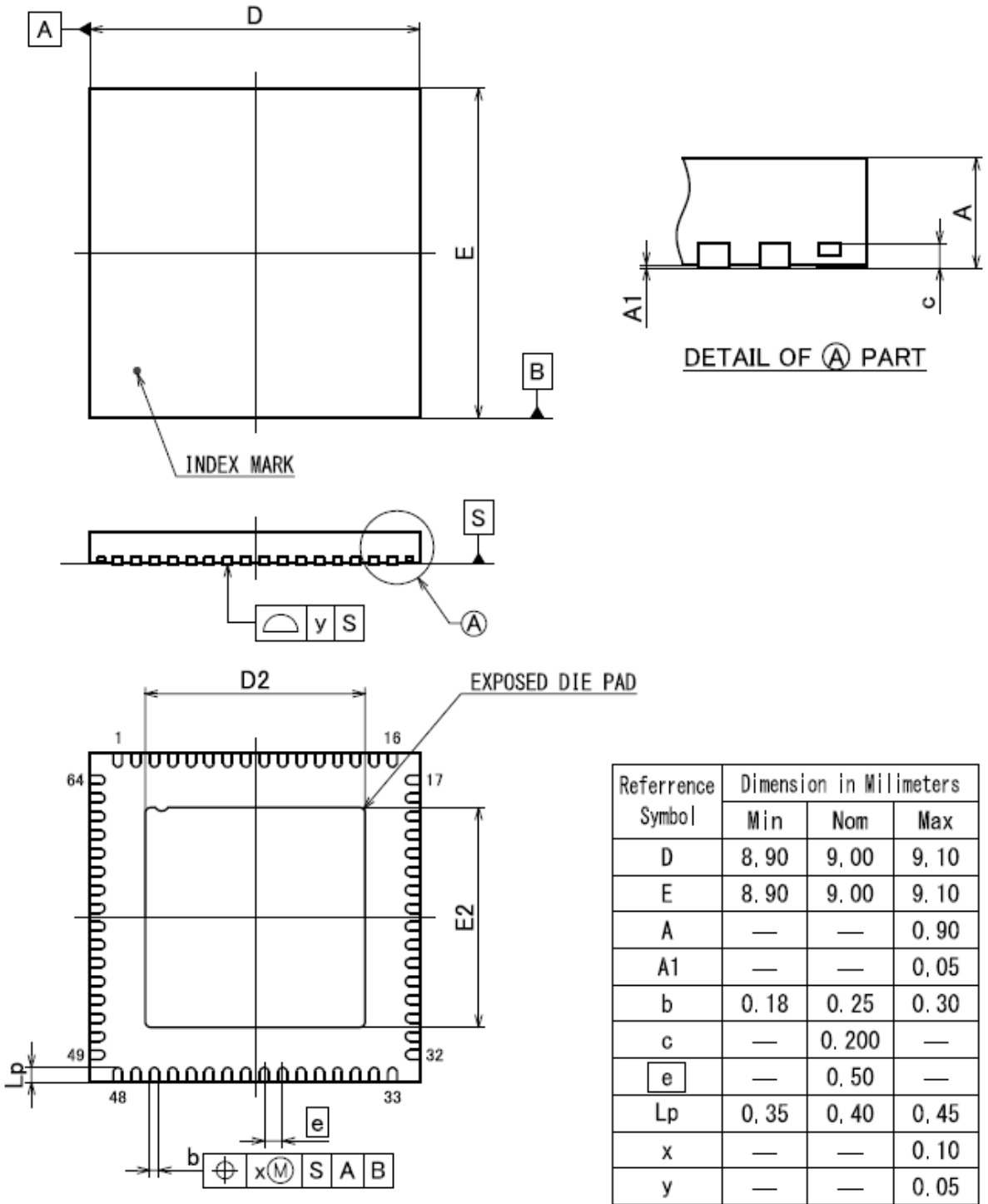
The phase detection function of various PLC protocols (G3-Cenelec/ARIB/FCC and PRIME1.3.6/ 1.4 etc.) is available by inputting the following Zero-crossing detection signal to GPIO2.



The rise time and fall times of the Zero-crossing detection signal including chattering time should be within 500us. After the rise of the signal, maintain a high level for 5ms or more. After the fall of the signal, maintain a low level for 5ms or more.

5. Package outline

JEITA Package Code	RENESAS Code	Previous Code	MASS [Typ.]
P-HVQFN64-9×9-0.50	PVQN0064KD-A	T64K8-50-BAS	0.21 g



Referrence Symbol	Dimension in Milimeters		
	Min	Nom	Max
D	8.90	9.00	9.10
E	8.90	9.00	9.10
A	—	—	0.90
A1	—	—	0.05
b	0.18	0.25	0.30
c	—	0.200	—
e	—	0.50	—
Lp	0.35	0.40	0.45
x	—	—	0.10
y	—	—	0.05
D2	5.90	6.00	6.10
E2	5.90	6.00	6.10

6. Part number

R9A06G037GNP#AA0

7. Appendix

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